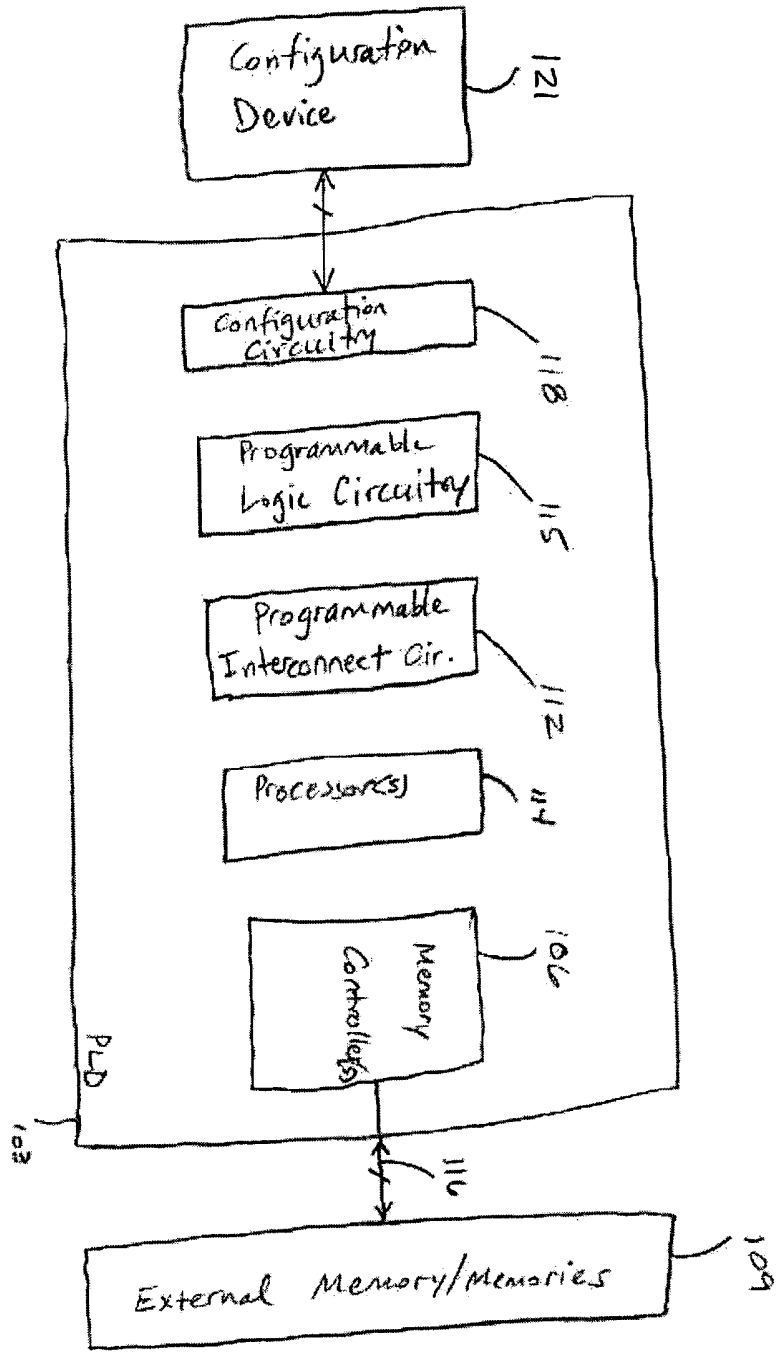
Configuration Device
121
Configuration Circuitry
118
Programmable Logic Circuitry
115
Programmable Interconnect Cir.
112
Processor(s)
114
Memory Controller(s)
106
PLD
102
110
External Memory/Memories
108

FIG. 1

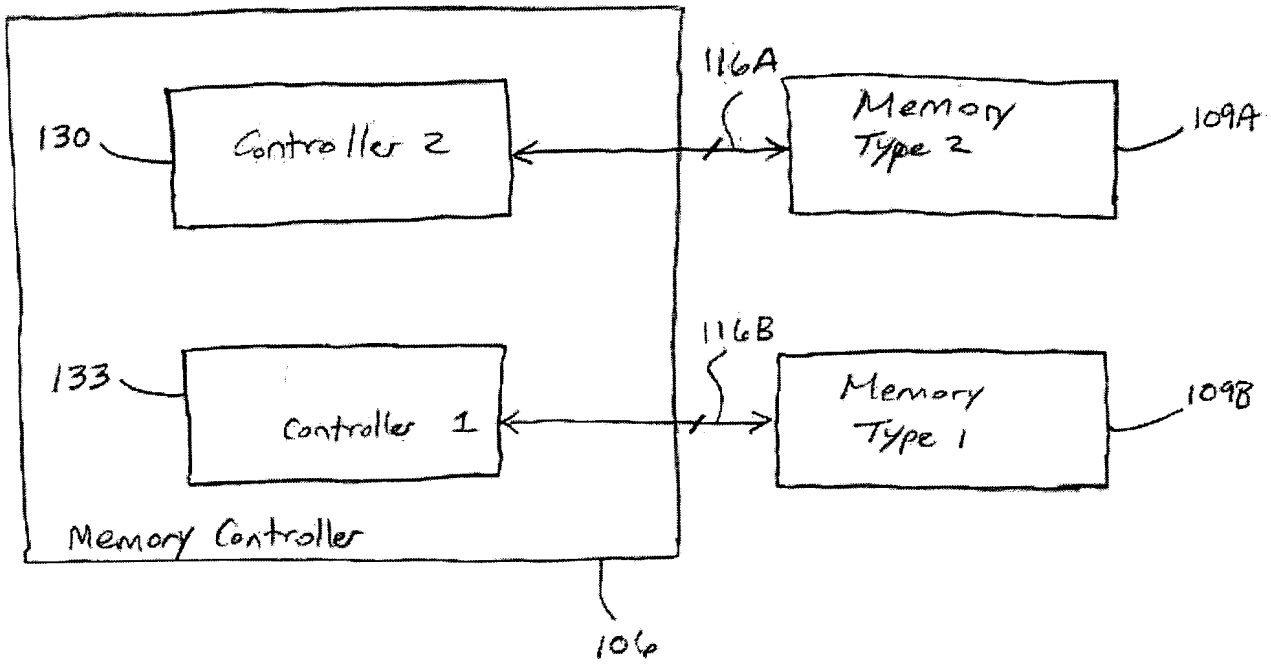
116A
130
Controller 2
Memory Type 2
109A
116B
133
Controller 1
Memory Type 1
109B
Memory Controller
106

FIG. 2

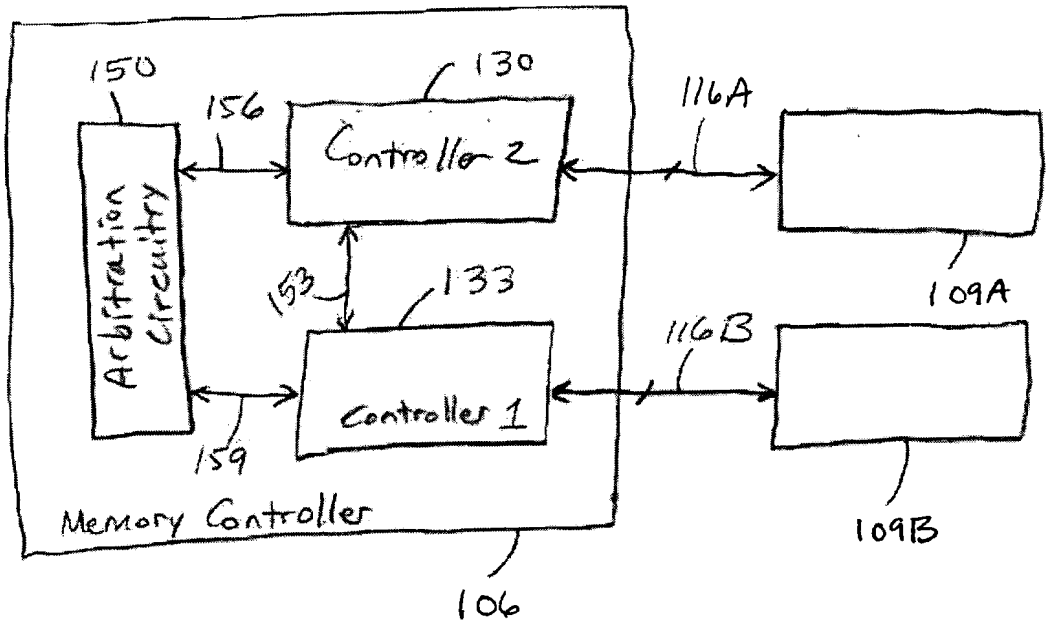
150
156
130
116A
Arbitration Circuitry
Controller 2
153
133
109A
116B
Controller 1
159
Memory Controller
109B
106

FIG. 3

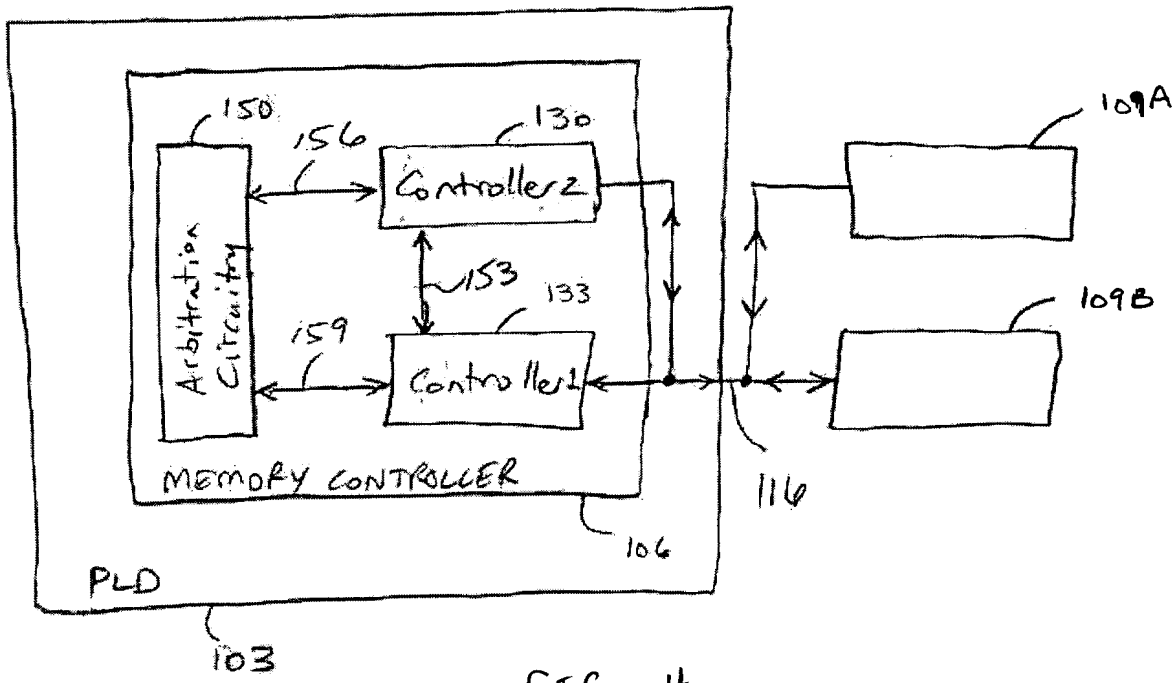
150
156
130
Controller2
153
133
159
Controller1
Arbitration Circuitry
MEMORY CONTROLLER
106
PLD
103
116
109A
109B

FIG. 4

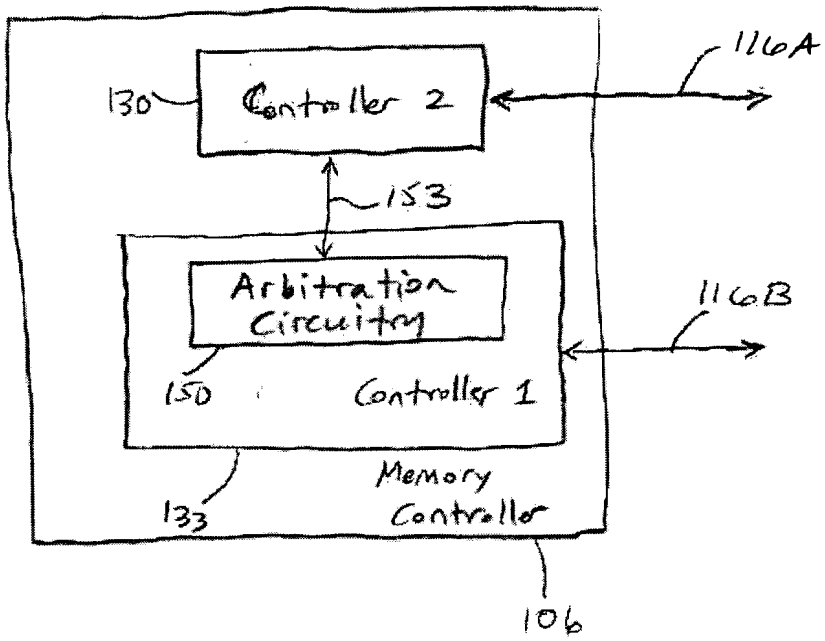
116A
130
Controller 2
153
Arbitration Circuitry
116B
150
Controller 1
133
Memory Controller
106

FIG. 5

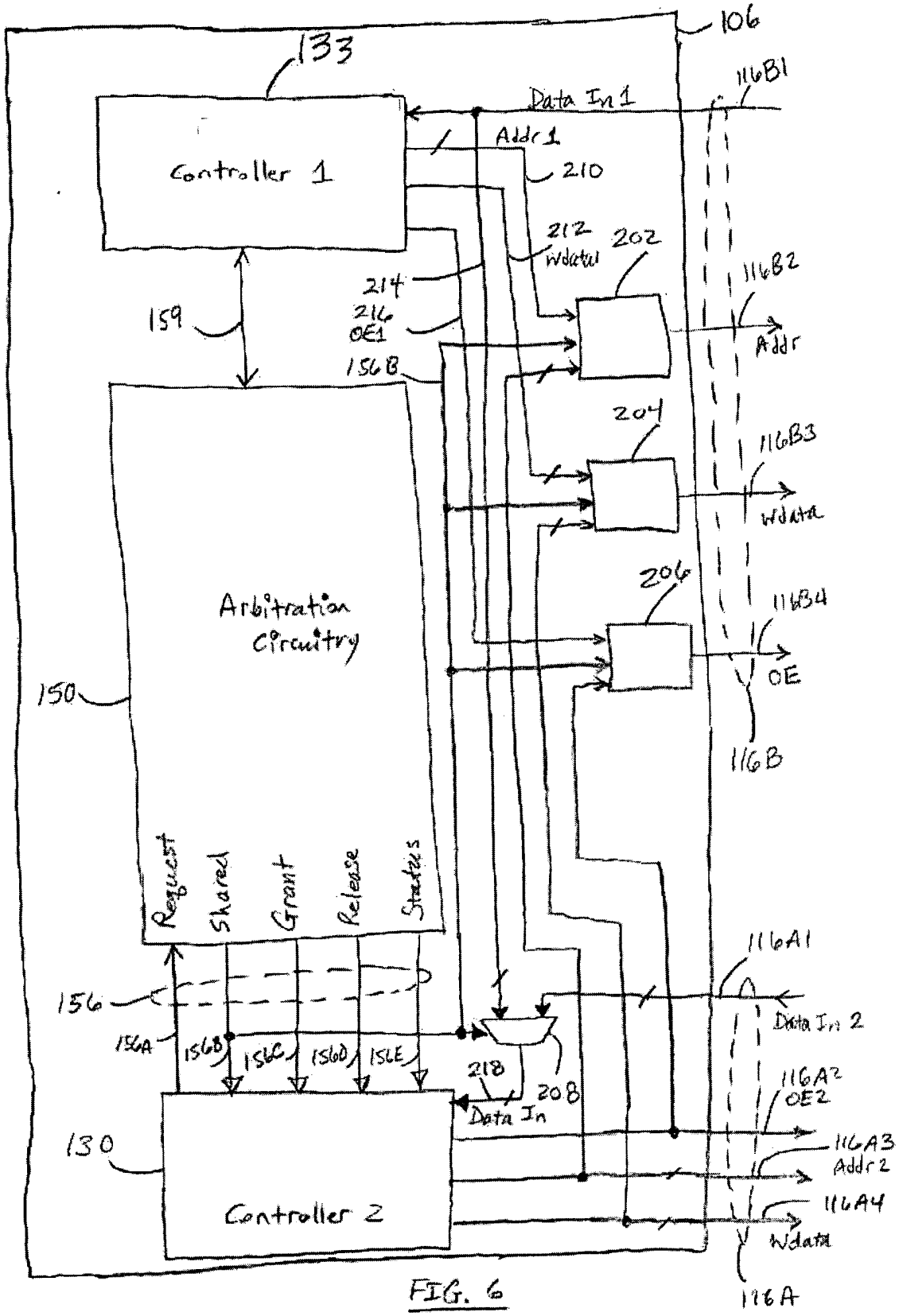
106
133
Controller 1
Data In 1
116B1
Addr 1
210
212
Wdata1
202
214
216
OE1
116B2
Addr
159
156B
204
116B3
Wdata
206
116B4
OE
Arbitration Circuitry
150
116B
Request
Shared
Grant
Release
Status
116A1
156
Data In 2
156A
156B
156C
156D
156E
218
208
Data In
116A2
OE2
130
116A3
Addr2
Controller 2
116A4
Wdata
116A

FIG. 6

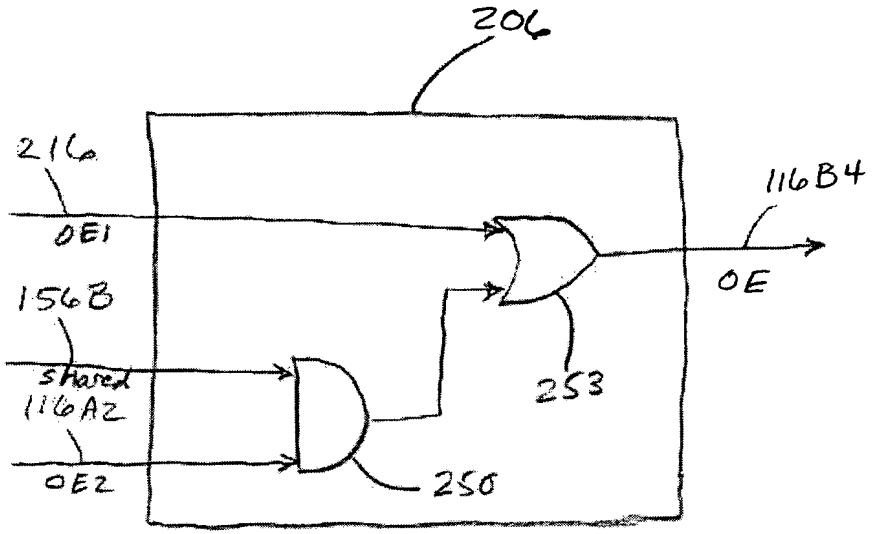

FIG. 7

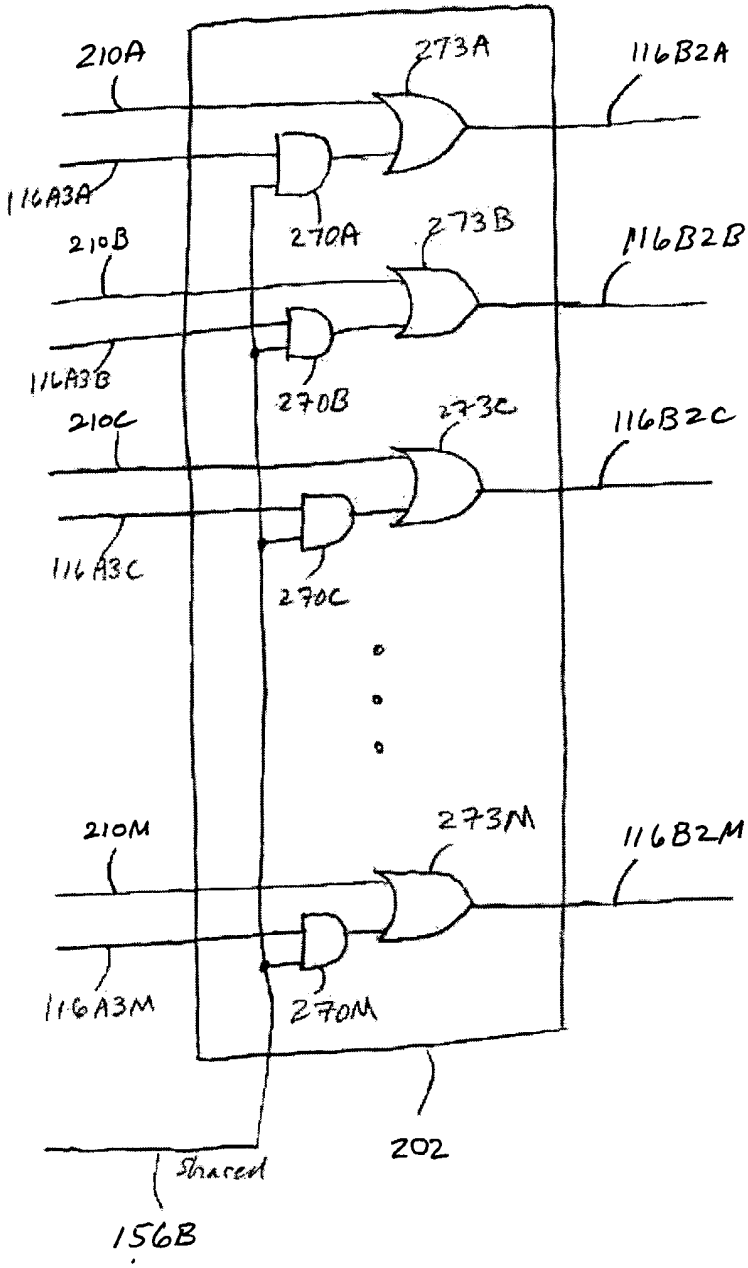
210A
273A
116B2A
116A3A
270A
210B
273B
116B2B
116A3B
270B
210C
273C
116B2C
116A3C
270C
210M
273M
116B2M
116A3M
270M
202
Shared
156B

FIG. 8

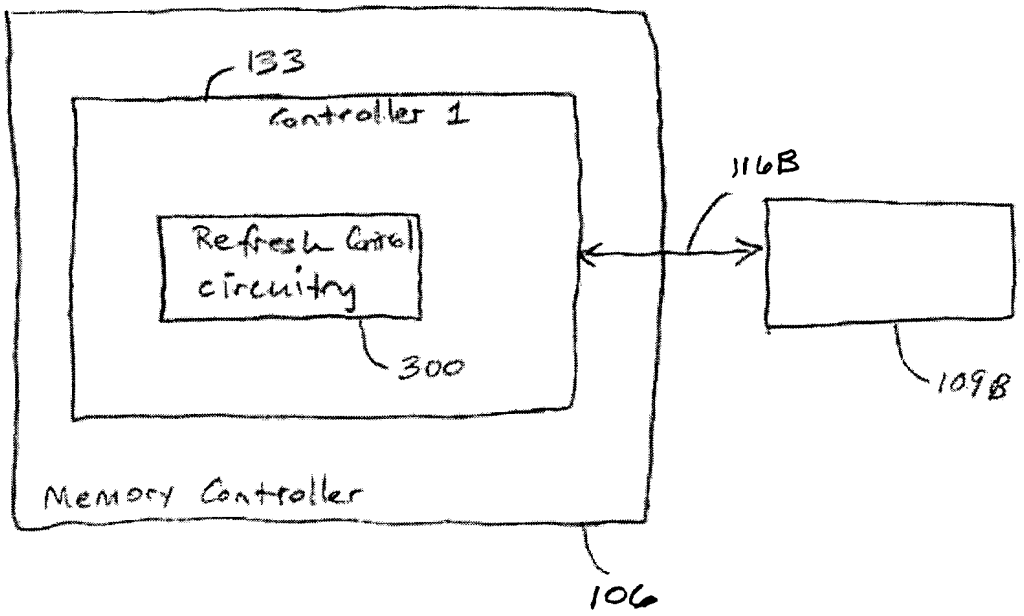
133
Controller 1
Refresh Cntrl
circuitry
300
Memory Controller
106
116B
109B

FIG. 9

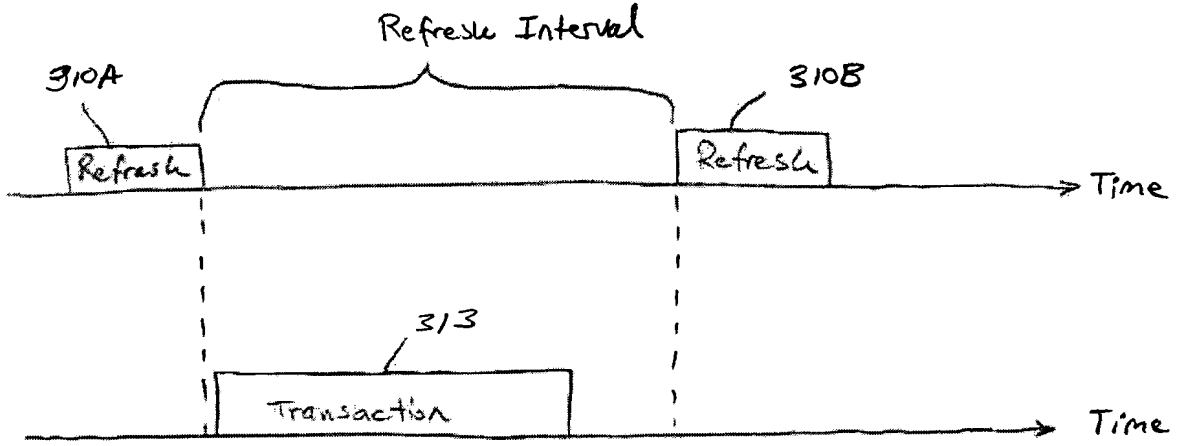
Refresh Interval
310A
310B
Refresh
Refresh
Time
313
Transaction
Time

FIG. 10

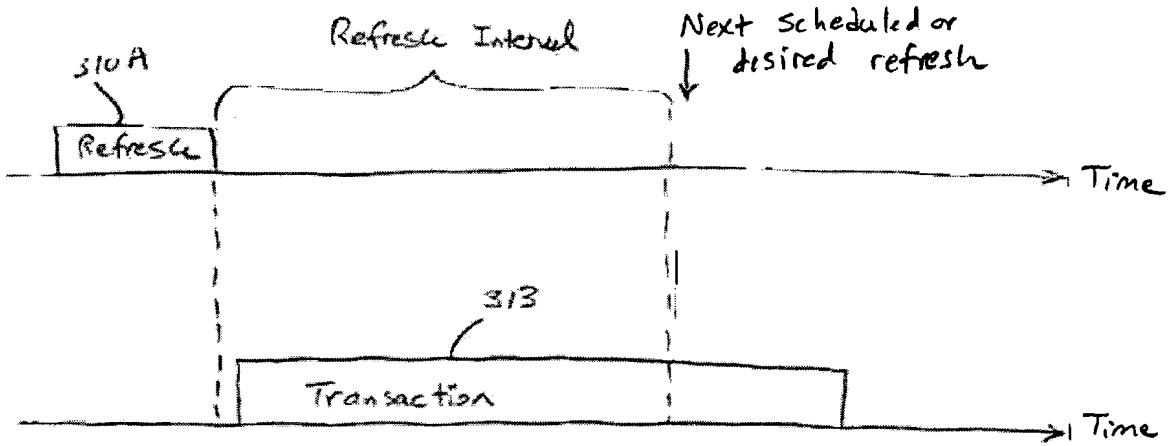
Refresh Interval
Next scheduled or desired refresh
310A
Refresh
Time
313
Transaction
Time

FIG. 11

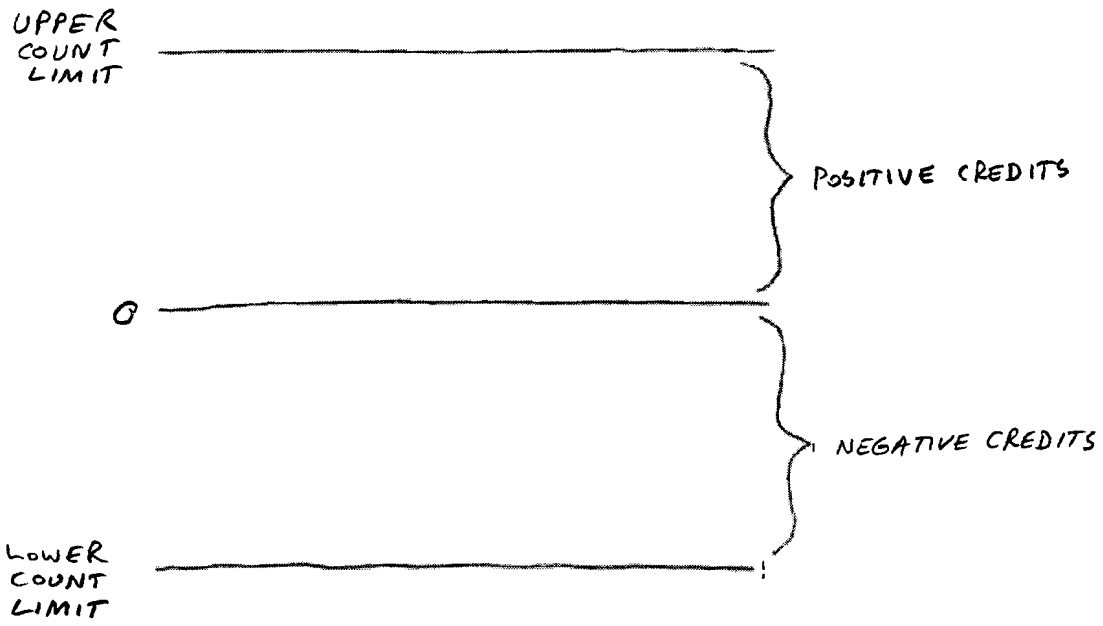
UPPER
COUNT
LIMIT
POSITIVE CREDITS
0
NEGATIVE CREDITS
LOWER
COUNT
LIMIT

FIG. 12